NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

PROTOTYPE DESIGN FOR NPSAT
VISIBLE IMAGER

by

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June 2000

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ABSTRACT *(maximum 200 words)*

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427.8 nm, 470.9 nm, 557.7 nm, 630.0 nm, 636.4 nm, and 844.6 nm.

    A Kodak 763 X 512 CCD was implemented into a push-broom scanner design appropriate for our mission. Design optics are for a nominal F/2, 90 mm Leica lens. The prototype was completed and demonstrated to operate.

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**PROTOTYPE DESIGN OF NPSAT
VISIBLE IMAGER**

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I. INTRODUCTION

A. BACKGROUND

The Naval Postgraduate School, in an effort to build upon its successful PANSat program, is developing a follow on satellite. This aggressive second-generation satellite vastly expands upon the groundwork laid by its predecessor. The bus is designed to carry multiple imaging systems into low Earth near polar orbit in order to collect scientific data on the Earth's aurora, the upper atmosphere, and the Earth's surface. A byproduct of this construction is invaluable hands on experience in every facet of satellite design, fabrication, testing, integration, and on orbit operation.

The preliminary design for the bus was mostly the work of Naval Postgraduate School Space System Engineers enrolled in the AA4871 Spacecraft Design II class. The results of this design [Ref. 6], and the concept of operation derived from it, provide the constraints and mission requirements of the payload imagers it will carry on orbit. These constraints drive the design and concept of operation of those devices.

B. PURPOSE

As a continuation of the satellite building philosophy, the visible imager payload for the NPSat is going to be developed in house at the Naval Postgraduate School. This will provide more experience for students while lowering the overall cost of the system and the satellite.

This thesis describes a prototype design for the visible imager and an exploration of the concept of operation of that system. It is the groundwork for follow on development and testing of the imager. This thesis will explore the pros and cons of the various hardware and software elements necessary to the development of an imager, and make recommendations as to final configurations where applicable. This design is complicated by the large dynamic range associated with the capability of imaging the daylit Earth and the relatively dim aurora.

The final goal of this thesis work was to construct an operational desk-top prototype. This involved integrating COTS hardware with custom built hardware and software. This prototype will be used to validate new technologies and operational techniques. It will also contribute to valuable experience working with and operating the imager.

II.   RECOMMENDED DESIGN SPECIFICATIONS

A simple, straightforward design is the goal for the visible imager. It has been designed as a complement to the primary mission payload, a thermal IR imager. The primary factor that makes it unique is an ability to work at low light levels, in order to image the aurora. The constraints that drive the design of the imager are as follows:

A.   CONSTRAINTS

Orbital Altitude	500 km – 1000 km (kilometers)
Orbital Inclination	$i > 75°$, not sun synchronous
Spatial Resolution	100 m (meters)
Spectral Resolution	10 nm (nanometers)
Spatial Coverage	50km
Spectral Coverage	500 – 900 nm
Mass	5 kg (kilograms)
Dimensions	12 cm Diameter X 20 cm Length
Power	10W (watts)
Data Rate	400kBps (kilobits per second)
Pointing Accuracy	1°
FOV	$\pm 2.9°$

Table 1. Constraints on the Imager. After Ref. [6]

The altitude was chosen based on a desire to pursue a fairly high resolution imaging mission. The low altitude constraint is due to atmospheric drag limiting time in orbit. The upper constraint is limited by launch vehicle and is the important value as far as the imager design is concerned. This altitude along with the required spatial resolution drives the size of the optics. Additionally the altitude controls the apparent ground speed

of the satellite. This speed, once again, along with the required spatial resolution will drive the sampling rate for the imager.

The inclination is a result of the type of data to be collected. High inclination is necessary to allow the imager to see the aurora. A sun synchronous orbit, however; is not desired because the nature of the aurora varies with local time. Imaging the auroral bands at different relative times of day (see Fig. 1) allows a better picture auroral dynamics.
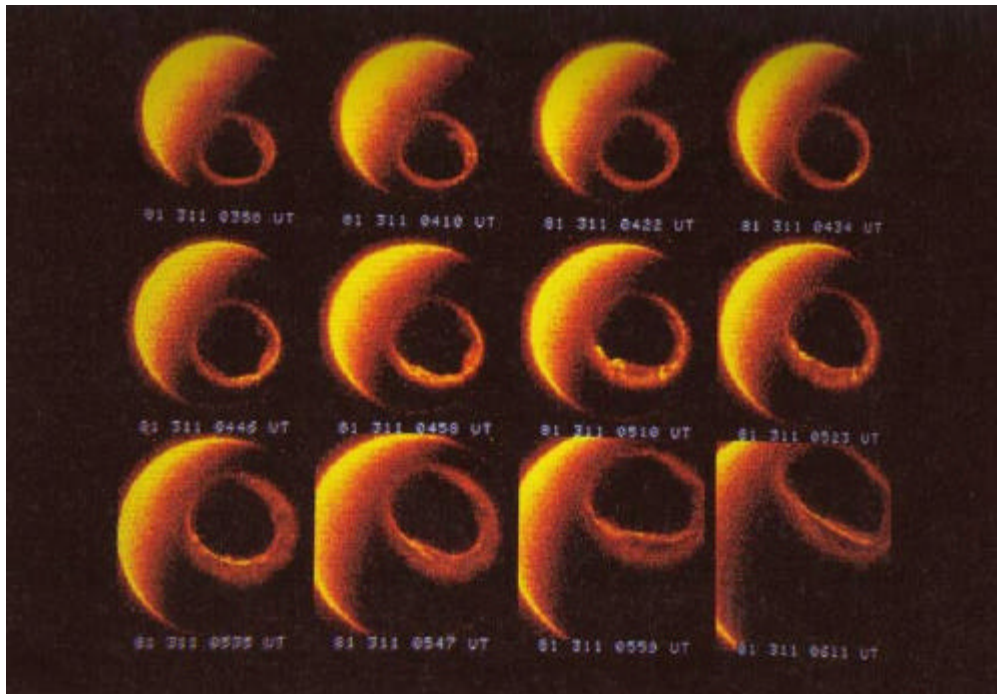

Figure 1 The Aurora at Different Local Times.
From Ref. [3]

The stated goal of the imager is 100 m spatial resolution. If met it will provide more detailed images of the structure of the auroral bands than have previously been achieved (Fig. 2). As stated above this resolution is a driving factor for the size of the optics and the refresh frequency of the imager. Higher resolution requires larger optics and a faster refresh rate.
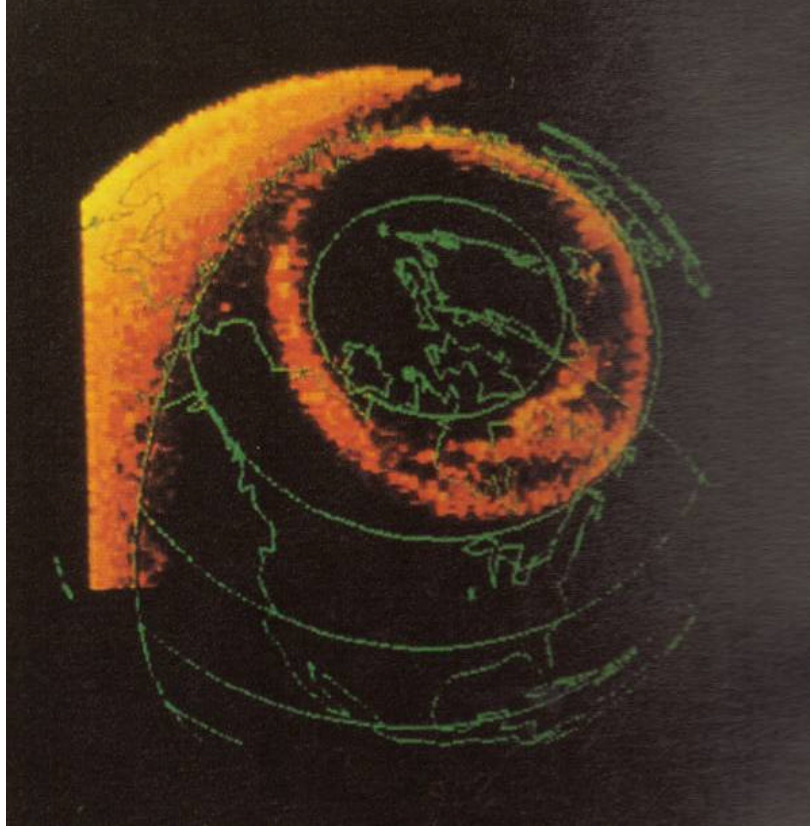
Figure 2 Auroral Image from Ref. [3]

Spectral resolution is nominally 10 nm; a value sufficient to resolve typical atomic features in the visible aurora. A spectral resolution of 10 nm is easily achieved with modern filter techniques [Ref. 15]. Targeting narrow bands makes it easier to identify what the radiation is coming from and consequently where and how it is being emitted.

The rest of the formal parameters like mass and dimensions only have a small impact on the prototype stages of the design. Power requirements need to be kept in mind, but solid state devices are usually easy on power. The concepts of operation can be tailored to meet the maximum data rate specification further along in the design. This is done by changing things like imager sensitivity and duty cycle times.

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B.   FILTER DESIGN AND SPECIFICATIONS

The filter allows the target frequencies of data to be recorded while clutter and other light frequencies can be excluded. In addition, recording data at separate frequencies allows this data to be recombined later to form a color image from what is actually a monochromatic imager.

Filtering is ideally suited to recording light from the aurora. As opposed to black body radiation, which is emitted in a continuum, auroral light is emitted in discrete frequencies. The photons are emitted due to electron transitions from excited to less excited or ground states [Refs. 1-3]. Each frequency is characteristic of a different elemental constituent of the atmosphere, and each element has multiple transitions it can make and therefor multiple frequencies it can emit.

1.   Spectrum Considerations

The primary concern in selecting spectral bands for the design was the requirement to image auroral red and green spectral lines. A high sensitivity blue band is useful for naval applications, and NIR is useful in looking at land surfaces. Combining the red, blue and green lines allow a color image to be created. Detailed considerations follow:

As seen in Figs. 3-4, the 557.7 nm atomic Oxygen line is the brightest line of the entire auroral spectrum. As a consequence, this line is the most often targeted when visible auroral data are taken. Choosing this line allows data taken to be compared to

previous observations for validity. This frequency is also a bright green that meets part of

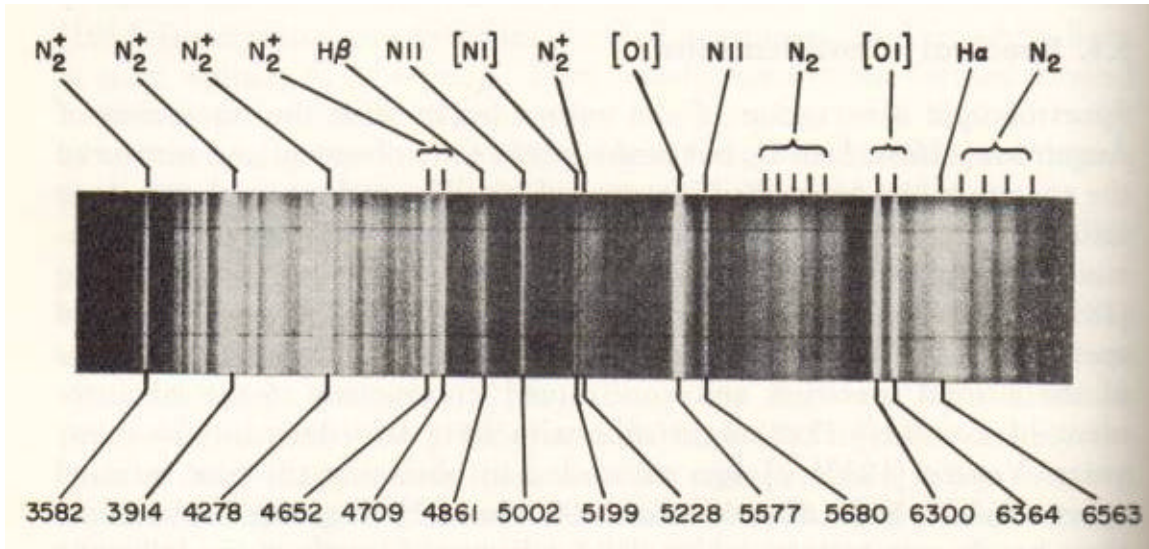the multi-spectral requirement mentioned above.

Figure 3. Auroral Spectral Lines. From Ref. [1]
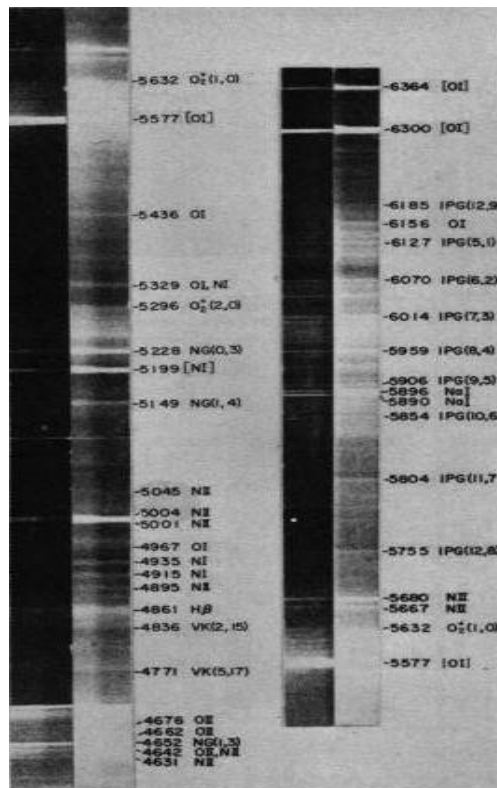
Figure 4. Auroral Spectral Lines. From Ref [1]

The 557.7 nm line also stands out from the clutter around it (Fig. 5), and would be well defined at 10 nm resolution.
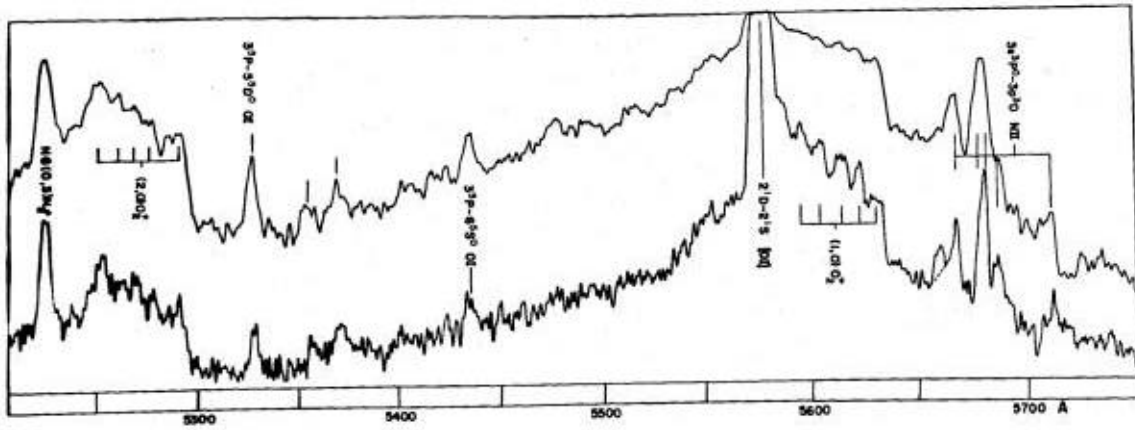
Figure 5. Auroral Intensity by Frequency. From Ref [1]

The two atomic Oxygen lines (Fig. 6) at 630.0 nm and 636.4 nm are good candidates for the red spectral line. Both lines are bright, and commonly used in auroral research.
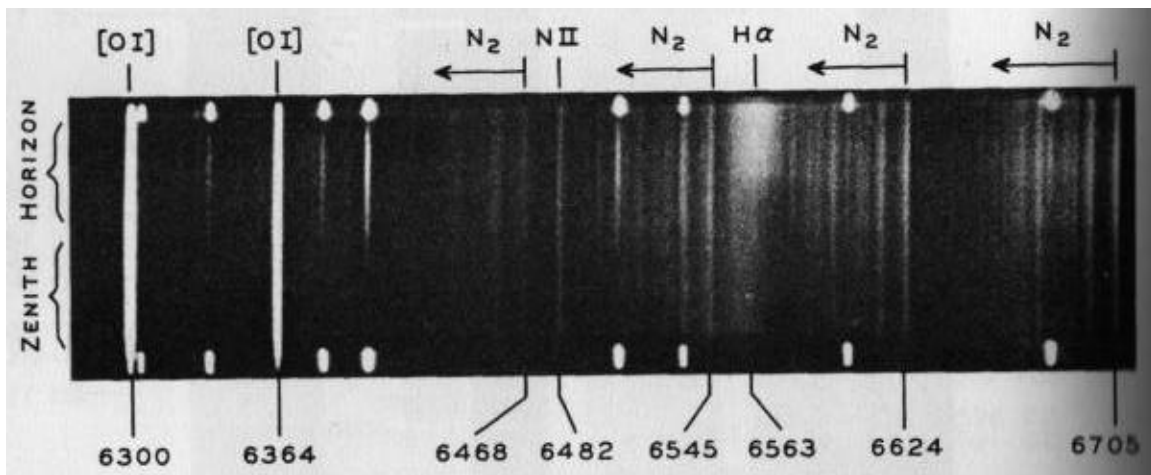
Figure 6. Auroral Spectral Lines. From Ref. [1]

The initial recommendation is for the 630.0 nm line because it is brighter, and can be more easily resolved from the surrounding clutter (Fig. 7). Other factors, however;

could make the 636.4 nm line a better choice. The distinction is not critical at this stage, as the imager design is not affected by the subtle difference.

Figure 7. Auroral Intensity by Frequency. From Ref. [1]

The best blue emission lines (Figs. 8 & 9) can be found at 427.8 nm and at 470.9 nm. These are both molecular ion (N_2^+) Nitrogen emission lines so can be contrasted with the Oxygen lines detailed above. The distinction between the contributions of the two species is an important element of basic auroral physics.

Figures 8 & 9. Auroral Spectral Lines. From Ref. [1]
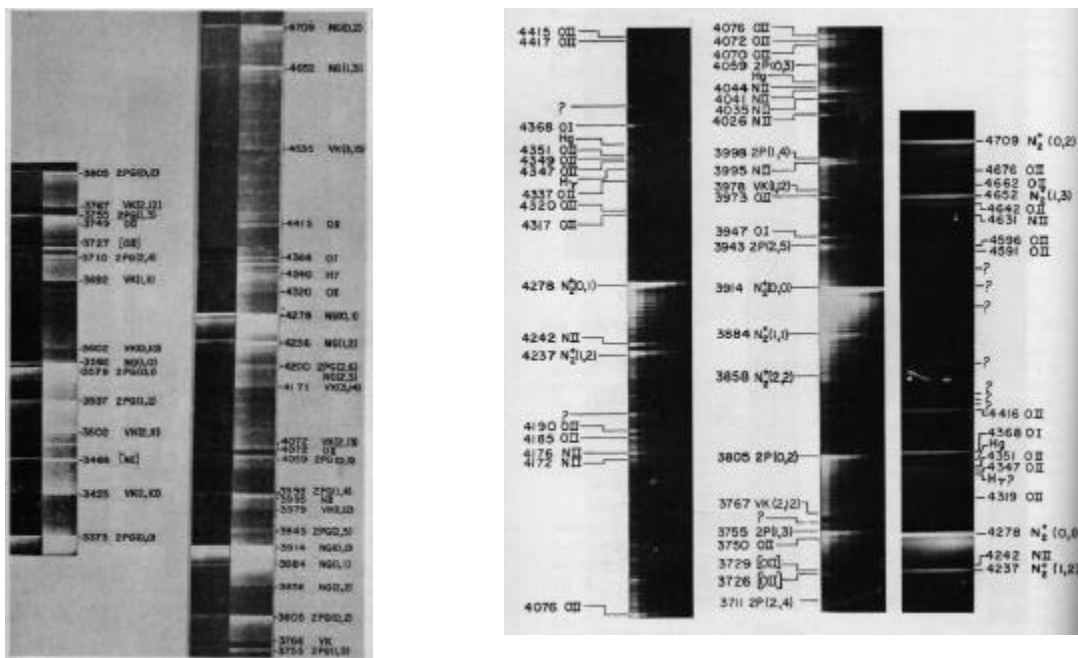
The 427.8 nm line would be brighter, and hence may be preferred, but other factors must be considered in this instance. Detectors respond differently to different frequencies of light. This is known as quantum efficiency. As seen in Fig. 10, typical quantum efficiency peaks near the center of the visible spectrum, and falls off to either side. For this CCD the peak is at 600.0 nm. At approximately 420.0 nm the quantum efficiency is 20%. The quantum efficiency at 470.0 nm is 25%. This loss of efficiency can make a significant difference in imaging dim scenes. In addition, some of the naval applications motivate additional bands in the blue. Multiple bands would allow sampling the band yielding the best data.
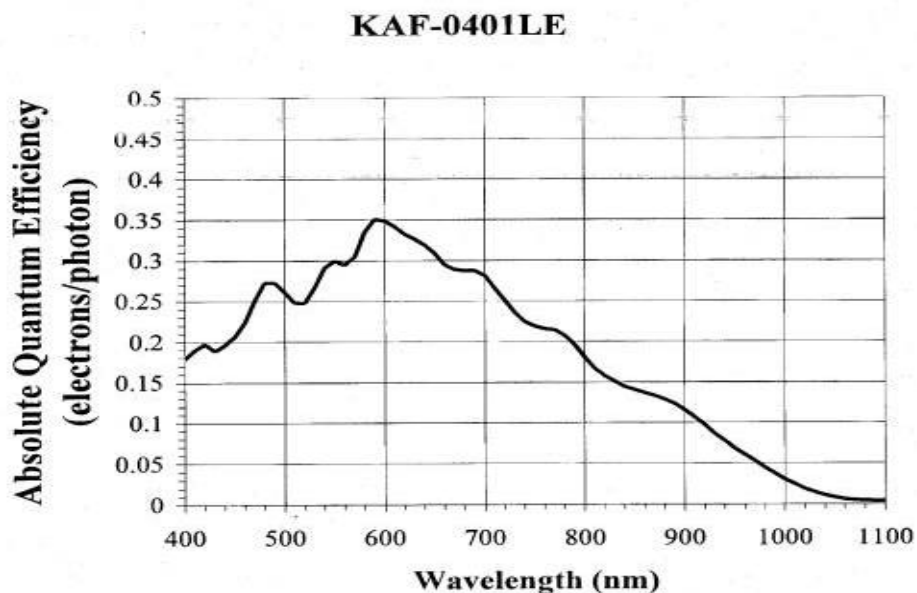

Figure 10. CCD Quantum Efficiency. From Ref. [8]

The near infra-red region (Figs. 11 & 12) does not offer many lines to choose from. There are a band of lines from 768.0 nm – 790.0 nm and a solitary line at 844.6 nm. None of these bands are terribly bright and therefor will tax the imager sensitivity.
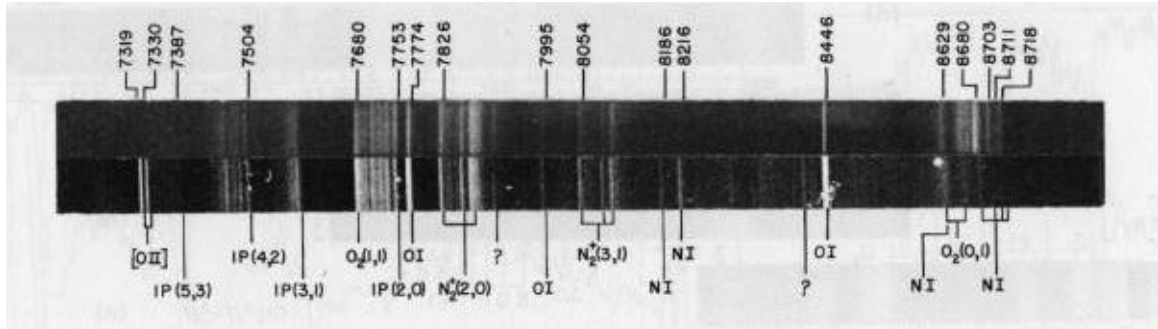
Figure 11. Auroral Spectral Lines. From Ref. [1]
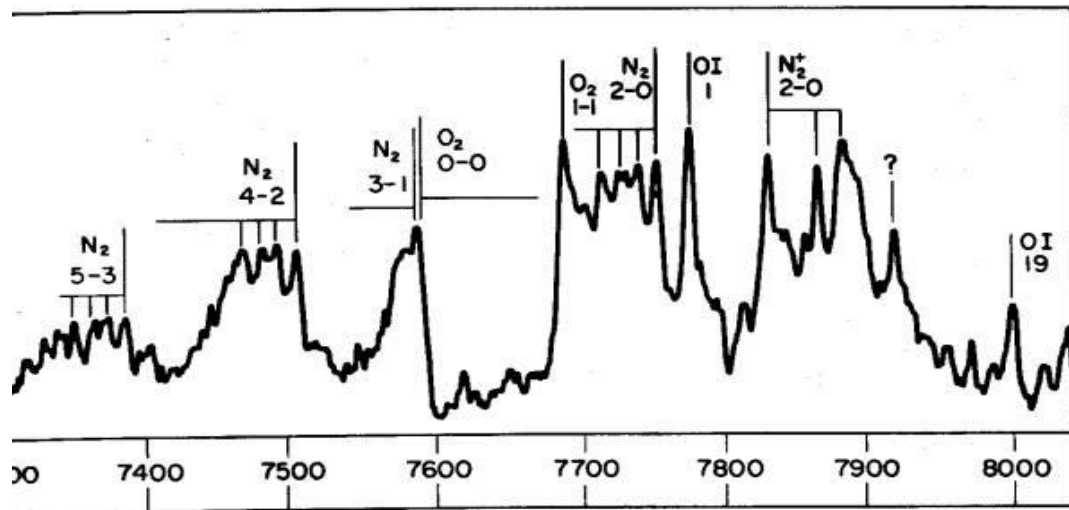
Figure 12. Auroral Intensity by Frequency. From Ref. [1]

The single line at 844.6 nm, an atomic Oxygen transition (Fig. 13), stands out against the background. Although this line suffers from a lower quantum efficiency, it still makes for a better target band.

In summary, the spectral frequencies the filter will be designed to are 427.8 nm and 470.9 nm in the blue, 557.7 nm in the green, 630.0 nm and 636.4 nm in the red, and 844.6 nm in the near infra-red. These will allow a reasonable sampling of the aurora as well as meeting the atmospheric and Earth imaging requirements. In operation, a subset of these bands will be used, along with a "wide open" or pan-chromatic band.
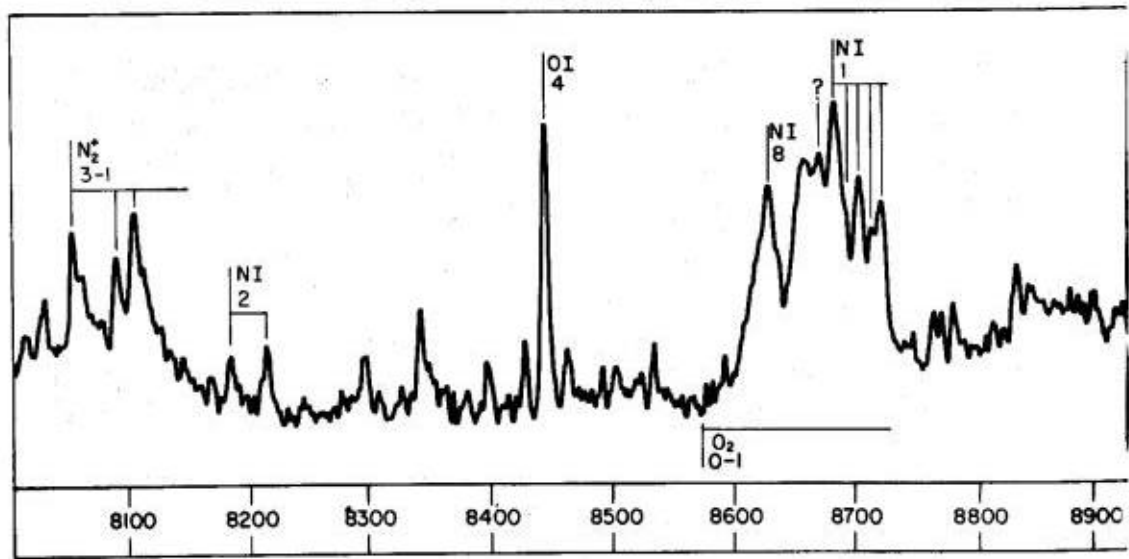
Figure 13. Auroral Intensity by Frequency. From Ref. [1]

2. Physical Design

Previous space imagers have generally used filter wheel designs that are relatively complex and heavy. Using a CCD array in a push – broom configuration provides the opportunity for another option. A 768 X 512 array is in effect 512 separate 768 pixels wide push broom arrays.

If separate filters could be laid against each other, directly over the CCD array then the first several lines of the array would be filtered to one frequency while the next several lines would be at another (Fig. 14).
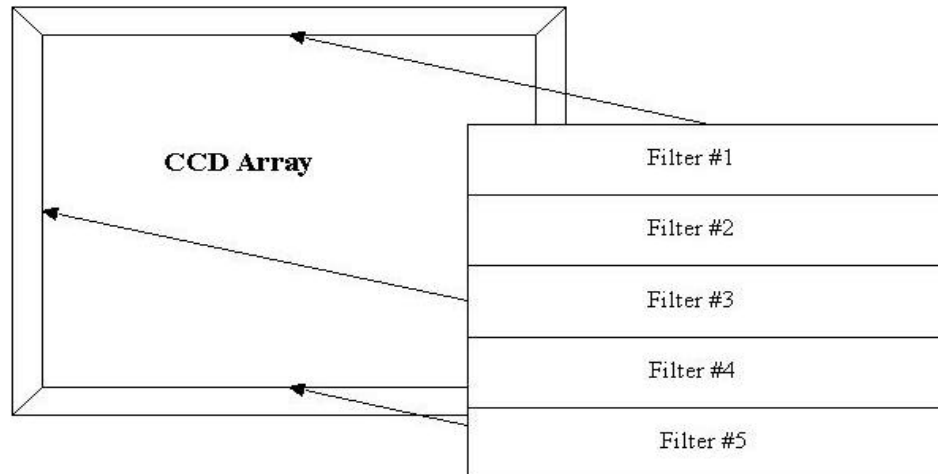
Figure 14. Composite Filter.

Optical Coating Laboratory Inc. makes a durable all-dielectric filter. The pass-band of these filters is fully selectable and meet the 10 nanometer spectral resolution requirement [Ref. 15]. This coating can be made to order for specific frequencies and deposited on the cover glass of the CCD array. A custom made composite filter covering the ranges specified would cost around $60,000 [Ref. 16].

Maintaining a sharp focus is a problem when changing conventional filters using a filter wheel. A similar problem exists with thin film filters. Different wavelengths of light have different path lengths and different refraction values when traveling through materials. This causes a focused image at one frequency to be out of focus at another. Due to the small thickness of the thin film filter this effect is minimized, however it can be further corrected by slightly thickening the glass on the lower frequency filters to match refraction across the composite filter.

C.   IMAGER

The two major categories of electronic imagers available are Charge-Coupled

Devices (CCD) and Complimentary Metal-oxide Semiconductor (CMOS) sensors

[Ref. 5]. The CMOS sensors are attractive for their low power consumption and size and

weight savings. CCD sensors are more sensitive. Because this sensitivity allows shorter

exposure or integration times, a CCD sensor can take more pictures in a given amount of

time than a comparable CMOS sensor. The orbital speed of the satellite, which limits the

imaging time available, combined with the relatively low intensity of light put out by the

aurora make a CCD imager the only viable option for the imager.

1.   Physical Dimensions

CCD sensors are a 2 dimensional array of pixels that come in a variety of pre-

designed sizes. A large array size allows for a larger field of view, but increases the

required data rate. The actual pixel size combined with the spatial resolution requirement

drives the size of the lens.

In general, CCD pixels average around 9 μm in size. Given an altitude of 1000

km and required spatial resolution of 100 m, from geometry (Fig. 15) the focal length is

90 mm. If the spatial resolution is 100 m, the array size in the horizontal direction sets the

swath width and consequently the field of view. Continuing the above example, a ground

resolution of 100 m combined with a CCD line length of 1024 pixels yields a swath width

of 102.4 km. The physical dimensions of the pixel on the CCD imager depend upon the

manufacturer and range from 8 μm to 15 μm. A larger pixel size requires a larger focal

length to maintain the same spatial resolution, whereas a smaller pixel size starts to impinge on the light gathering area.

$$F = \left(\frac{A}{R} \right) * P$$
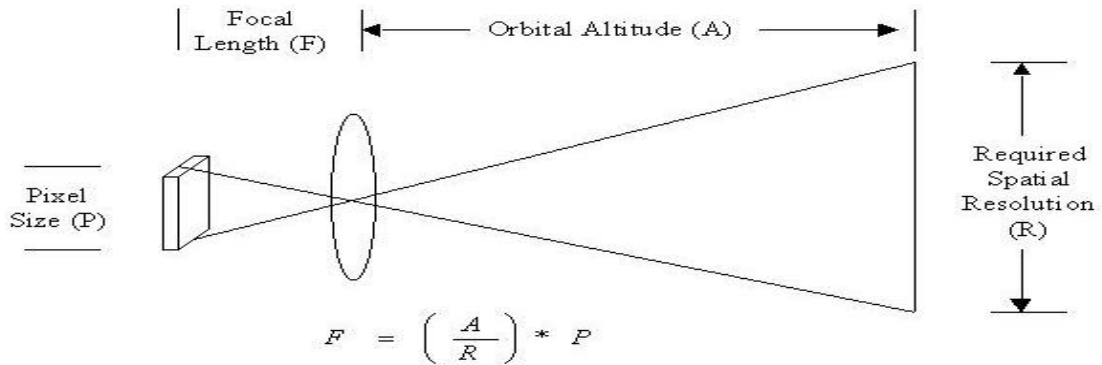
Figure 15. Geometric Optics.

2. Sensitivity

The sensitivity of the CCD imager is driven by two separate requirements. The imager must be sensitive enough to pick up the dim auroral lines, yet have enough dynamic range to be able to image the sun lit Earth. A good base line for brightness calculations is around 1000 Rayleigth or 1 kR. The 557.7 nm atomic Oxygen line gets as bright as 1000 kR [Ref. 1, pp. 571]. For reference, an adapted human eye can see as little as 3.5 x 10^{-4} R and the full moon is about 70 kR, while the daylit Earth is about 100,000 kR [Ref. 2, pp. 213].

1 Lux = 3.5 x 10^{11} photons/cm^2-sec = 3.5 x 10^5 Rayleigh = 350 kR

[Ref. 1 pp. 569, Ref. 2 pp. 213]

The background noise or dark current for a CCD imager is around 30 electrons/pixel/second [Ref. 9]. Doubling this value to 60 e/p/s will give a level that

stands out from the background. The average quantum efficiency of CCD devices is approximately 25% [Ref. 8]. This means 240e/p/s are required to create the baseline level at the CCD output. A filter efficiency of 60% [Ref. 15] means 400 e/p/s are required to create the baseline level. Each pixel is 10 μm across with an area of 1×10^{-6} cm^2. Converting from pixel to area yields 4×10^8 e/cm^2/s. This converts to .4 kR. This means that using a 1 milli-second integration time for the CCD array, the dimmest band that could be resolved is 40 kR. The fainter auroral bands will not be visible without additional help. More complicated techniques, as detailed below, will need to be used. The primary will be a form of Time – Domain Integration (TDI) will be used.

3.   Speed

The imager is under a time constraint due to its motion in orbit. A 1000 km orbit yields a ground speed of 7.35 km/s. If the spatial resolution is 100m the imager will cover that distance in 13.6 ms. This is the time limit the imager has to work with. Data output speeds of the typical CCD imager are upwards of 10 MHz [Ref. 8] which are more than fast enough to remove 5 lines of 1024 pixels. Integration time takes up most of the time allotted. The longer the integration time the more chance the CCD has to gather photons. If an integration time of 10 ms is applied to the above example 40 kR would be necessary to register above the noise floor. This value is becoming large with respect to the average brightness of an aurora.

A way around this integration time problem is through binning. If, instead of clocking a pixel out once it has seen its place on the ground, it is clocked down one line in the direction of motion of the satellite, it will get another look at that piece of ground.

This effectively doubles the integration time. The pixel could be binned through all the lines on the CCD covered by its filter. This would increase the sensitivity of the imager while staying within the time constraint. The only caviat to this technique is that in order to maintain complete ground coverage, a block of lines equal to the amount of binning plus one would need to be followed. For example: If 3 lines of binning are required, lines 1-4 would step down 3 steps to become lines 4-7. They would need to be clocked out between steps 3 and 4 to allow the new lines 1-4 to be binned, and get clocked out in their turn. In this way, 3 lines of binning require 7 lines on the CCD (see Fig. 16).

Flight direction

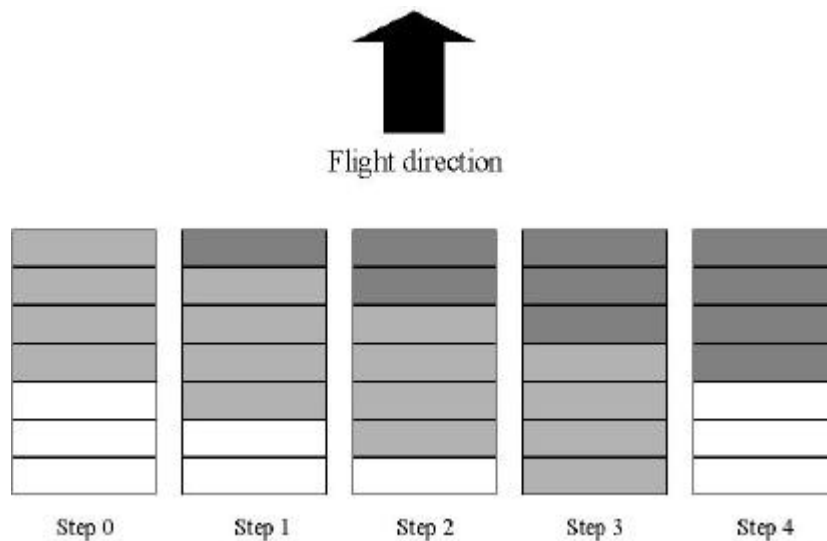Figure 16. 4 Line Binning Mode with 3 TDI Steps.

D.   OPTICS

The lens is the defining part of any imaging system. A custom built lens would be ideal, but is out of this project's price range. The University of Surrey has done testing of a variety of commercial off-the-shelf lenses [Ref. 4]. They had good luck with several European brands and have flown several Leica lenses with small modifications.

The biggest thing to look for when evaluating a lens for space worthiness is the use of non-space compliant materials. Plastics, rubber, nylon and many types of adhesives don't handle the vacuum of space well. In most cases these can be replaced or just removed. The mechanical strength of the lens is the next thing to be evaluated. In order to stand up to launch stresses a lens needs to be conservatively designed. This goes against the design goals of many commercial lenses. These try to achieve smaller and lighter structures to increase the portability of their systems.

Once a type of lens is chosen, a test lens needs to be purchased. Initial tests for this lens will include performance specs to make sure it will meet the needs of the project. The follow on tests will require the destruction of the lens. Manufacturers are understandably wary of giving out detailed construction specifications. The only way to be sure of the parts and materials use in the lens is to totally disassemble it. In the course of this disassembly, a list of parts to be removed or replaced can be created and experience on how exactly to go about removing or replacing without damaging the lens can be compiled. This procedure has been used successfully by the University of Surrey. [Ref. 4]

1. Size of Lens

A lens is generally characterized by the focal length and F/stop #. The focal length denotes the curvature of the lens and the F/stop # is the ratio of the focal length to the lens diameter. The F/stop # is a measure of the resolving and light gathering properties of the lens.

The focal length of the lens can be calculated using simple geometric optics. Given the sensor altitude of 1000 km, the spatial resolution of 100 m and the pixel size of 9 µm, the focal length is computed to be 90 mm.

The minimum diameter of the lens is a function of the Rayleigh criteria.

$$D = \frac{(1.22)lR}{\Delta x}$$

R = 1,000,000 m and is the altitude of the imager. λ = .8 ee –6 and is the limiting spectral

$$F \ / \ \text{stop} \quad \# \ = \ \frac{F}{D}$$

line wavelength. Δx = 100 m and is the spatial resolution constraint. With the above values D is calculated to be 9.76 mm. To put this in terms of F/stop #:

Since F = 90 mm and D = 9.76 mm, the Rayleigh criteria is met with any F/stop # less than 10. Most lenses of this size have apertures of better than F/5 and the Leica 90 mm lenses considered have apertures from F/2 to F/3. The larger apertures of these lenses increase the number of incident photons on the imager surface, thereby increasing the sensitivity of the imager by a significant factor.

2.   Focus Requirements

The traumatic launch followed by severe thermal shifts while on orbit make for a challenging environment to maintain the geometry of an imager. Even a small change in distance or alignment would seriously degrade all data taken. Active and passive methods can be employed to maintain proper focus of the optical system.

Digital data along with the processors that handle the data provide the opportunity to generate feed back signals that will enable accurate refocusing of the optics while on orbit. This refocusing can be done continuously to maintain accurate geometry even during the thermal cycles involved while moving in and out of eclipse.

The feed back signal is generated by contrasting the difference between two adjacent or nearly adjacent pixels. If the contrast is greater after a small focus adjustment then another small focus adjustment in the same direction is tried. If the contrast is less, then a focus adjustment in the other direction is initiated. Ideally this is done with several pixel pairs in random places on the array. These values are averaged then used to produce the control signal.

While the concept of an auto-focus imager is simple, developing it would not be. The use of a COTS lens forces an auto-focus mechanism to operate the lens in a restricted, external way. A motor would need to be employed to operate the helical ring and change the location of the lens. This motor would seriously increase the weight and power required to operate the imager. A better solution would be to change the location of the CCD. Rails would allow motion along the imager axis while restricting other degrees of freedom. Shape memory alloys using small currents could be used to position the CCD and maintain its location precisely at the focus of the lens. Unfortunately, mounting electronics on a mobile platform subjects them, and the wiring that goes with them, to increased vibration. Without extensive testing this could easily prove fatal for the imager. While this may still prove to be a usable solution, given enough experimentation with the imager, it is not recommended for the initial system. The experience is not available to produce that ambitious a design on site.

The best method of ensuring proper focus is conservative design. The entire imaging package must be properly secured. The braces that maintain the spacing between lens and CCD must be thermally neutral. As the temperature of the material changes it should neither expand nor contract. In addition, a method should be provided of checking the focus during integration. This method should also be used to ensure proper focus before, during and after testing. This is the recommended design for the school's first space based imager.

E.   ELECTRONICS

Handling the data once it leaves the amplifier output of the CCD is the domain of the onboard electronics. These systems are usually custom designed to meet the specific requirements of the imager. They provide the surge storage, data processing and bulk storage until the satellite data handling system is ready for transfer.

1.   Processor

The processor controlling this imager will serve several functions. It will control the overall operation of the imager. This is a non-trivial task due to the many operational modes involved. These include multiple binning options and daylight versus auroral imaging. In addition, non-standard operation for error determination may become necessary.

The processor will also need to be able to handle large amounts of data at a reasonably fast speed. The data needs to be removed from the surge memory,

compressed, then placed in the long term storage to await transfer to the satellite bus. The processor must have the capacity to implement the image compression algorithms without choking the data flow.

The downside to fast processors is the number of upsets. Fast processors mean small and dense chips. These chips are more susceptible to upsets caused by radiation. These upsets can be as minor as corrupted data and as major as a locked up processor. A radiation hardened processor is at least an order of magnitude more expensive than a standard processor. Incorporating extra shielding into the imager design significantly increases the weight of the system.

UOSat-12 processes 20 Mbps using a 25 MHz non-hardened commercial processor [Ref. 4]. Their data rate is comparable to the expected data rate of the NPS imager. With minimal shielding the University of Surrey operated their imager without any major upsets. This validation of the concept provides strong support to an NPS design using a fast commercial processor.

2.   Memory

Due to the orbital speed of the imager, 73 lines of data per second need to be recorded to maintain continuous coverage. At 12 bits of resolution per pixel and 1000 pixels per line this equates to 100 kbytes per second of data. When all 5 spectral lines are being recorded 500 kbytes of data a second need to be stored. A 4 mbyte flash memory card would provide roughly 8 seconds of storage. This would be an ideal size buffer memory for the output of the CCD. This buffer memory is an important part of the data flow. Data leaves the CCD in spurts. 90% of the time the CCD is integrating, which

allows for no data flow. In the short time frame between integrations, all the data must be removed from the CCD. A surge or buffer memory would allow a processor to operate at the average data speed, instead of the much faster CCD rate.

Once the processor has completed data compression algorithms the data will go to the long term storage memory. This memory will store the data until the satellite data handling subsystem is ready for it. The data will then be transferred serially to the satellite onboard memory. The size of this memory is dependant on the cycle time of the data handling system of the satellite. The more often it is available for transfer, the smaller the long-term memory requirements will be. The size of this memory block can be scalable with little impact on the actual design of the imager.

3.   Hardware

There are several major pieces of hardware involved with making the imager function. The satellite will provide power to the imager at the bus voltage. The imager power supply will need to convert that voltage to those needed by the rest of the imager. In most cases that will be 5 V, however; for the CCD the voltages are 15 V and –10 V. Data from the CCD is an analog voltage from 0 – 3 V. An analog to digital converter (ADC) will need to be employed to put the data in a form the processors can handle. The ADC must have a cycle time fast enough to process the data without causing a bottleneck. This means upwards of 1 Mbyte per second. Current state of the art for ADCs is an order of magnitude faster than this rate [Ref. 7]. The ADC must also have enough sensitivity to enable it to pull the 60 e/p/s signal from the 30 e/p/s dark current noise. This

means it must have at least a 15 electron per A/D count setting. This sensitivity is also achievable with current ADCs.

A system clock will also need to be implemented. This clock will be involved in clocking data out of the CCD and synchronizing the data transferred between the various memories and the processor. This clock can be a part of the processor or its own entity. Many lower level electronic devices and logic circuits will also need to be implemented. Data needs to be moved and tracked from the ADC to the surge memory, then to the processor and finally to the long term memory. Logic gates to control the functionality of the major components must be built.

III.   BENCHTOP PROTOTYPE

In order to validate the directions taken during the design phase and to test technologies prior to implementing them, construction on a bench-top prototype was begun. The goal of the prototype is to use electronics that are identical or near identical to those that will fly on the satellite. During early stages, substitute equipment will be used to allow validation and testing of major techniques or electronics.

A.   KAF – 0401E

The Kodak KAF – 0401E full frame sensor was chosen as the CCD test platform for the prototype. This 768 X 512 pixel array device is part of a line of standard CCDs offered by Kodak. The advantage of this setup is that once the hardware has been designed the CCDs can be switched with very little if any modifications. Minor code changes are all that is necessary to store the different number of pixels per frame. Currently the final imager is specified to be a 1024 X 1024 imager. This is to meet the minimum swath width requirements. Kodak has developed larger CCDs, however data rate and storage restrictions preclude using them.

With the purchase of the KAF series Evaluation Board the school received 5 KAF-0401E CCDs. Two were classified C1 with less than 5 point defects and no column or cluster defects. Two were classified C0 with no point, column or cluster defects, and one was classified Engineering.
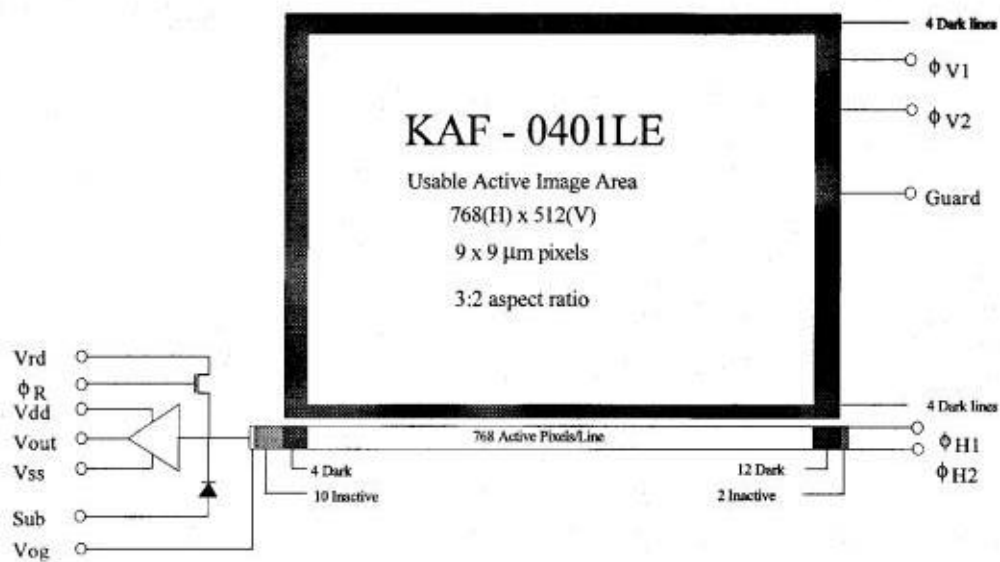
Figure 17. CCD Circuit Design. From Ref. [9]
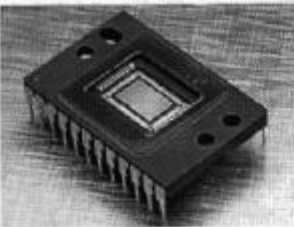
Figure 18. CCD Specifications. From Ref. [8]

In its final design configuration the CCD will operate in conjunction with custom designed hardware tailored to the mission. For the prototype, the CCD is designed to operate as a part of the KAF series Evaluation Board.

B.   EVALUATION BOARD

During prototyping, Kodak CCDs are designed to be controlled by the KAF series CCD Digital Reference Evaluation Board. (DREB) [Ref. 7]. The DREB is an integrated amalgamation of most of the hardware items necessary for running the CCD.

Figure 19. Digital Reference Evaluation Board Schematic.
From Ref. [7]

The DREB has onboard power conversion from a supplied 5 V to the 15 V and –10 V required by the CCD. The board's maximum speed is constrained by the ADC and is 12 bit parallel data 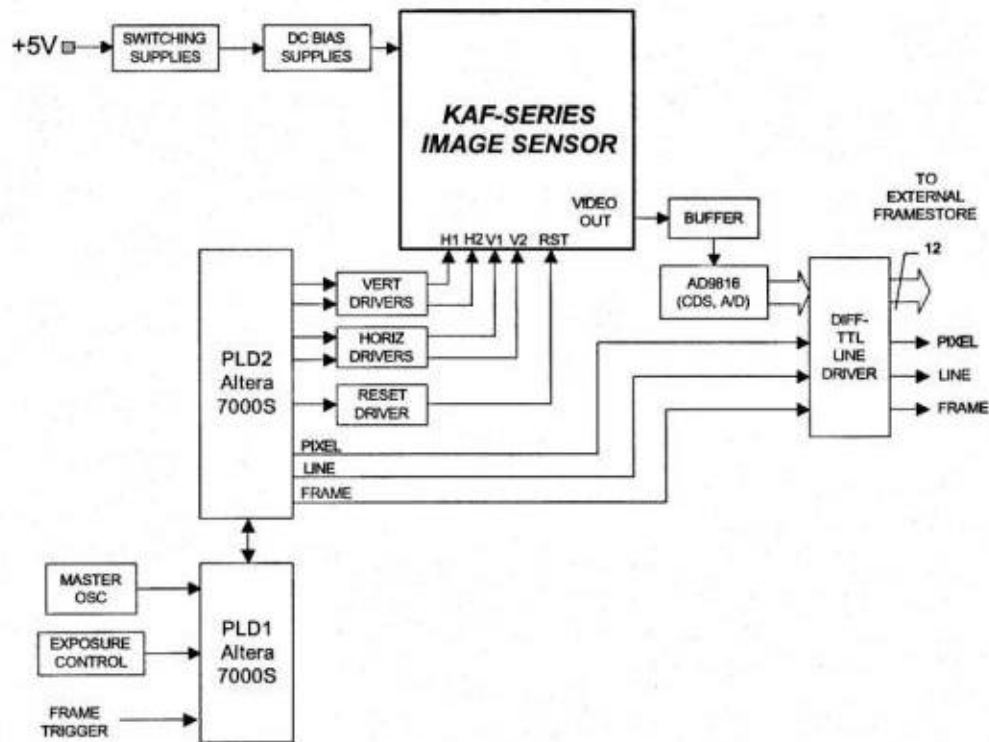at 6 MHz. The ADC sensitivity can be set as low as 12 electrons per AD count. This is below the 15 electrons per AD count limit detailed above. The board comes with a 40 MHz master clock that is used to synchronize all on board functions. The Board outputs 12 lines of data and 3 frame grabber control signals in RS422 differential TTL format. This allows for twisted pairs to reduce the amount of cross-talk during data transfer. The frame grabber control lines are Pixel, Line and Frame. The board also provides an integration signal to allow automatic operation of a shutter during integration.

Most board inputs can be implemented using on board switches or control line signals. Standard integration times can be set from 10 ms to 10 s @ 40 MHz clock speed. A slower clock speed means longer integration times. The DREB has preprogrammed binning modes that go from 1 X 1 to 10 X 10.

C.   PROCESSING AND DATA STORAGE

A modern PC has all the capabilities and processing power needed to meet the requirements of a benchtop prototype imager. It can send control signals. It can collect and store the data. It can process the data and display it in a variety of formats depending on the software available. Having a single machine cover all those functions greatly simplifies the work area. As the prototype evolves, the PC will be phased out until it only fills the functions of data handling equipment beyond the imager.

The PC used in the lab is a 266MHz machine. It contains 384 Mbytes of RAM and a 4 Gbyte hard drive. The high clock speed and large amount of RAM make this computer ideally suited to process large image files. In addition, the hard drive is large enough to provide storage space for a number of image files.

D   IMPLEMENTATION

1.   Electronics

Several things needed to be done to the data that leaves the Evaluation board before it is ready for imputing into the computer. This processing is set up on an intermediate prototyping board (see Fig. 20).
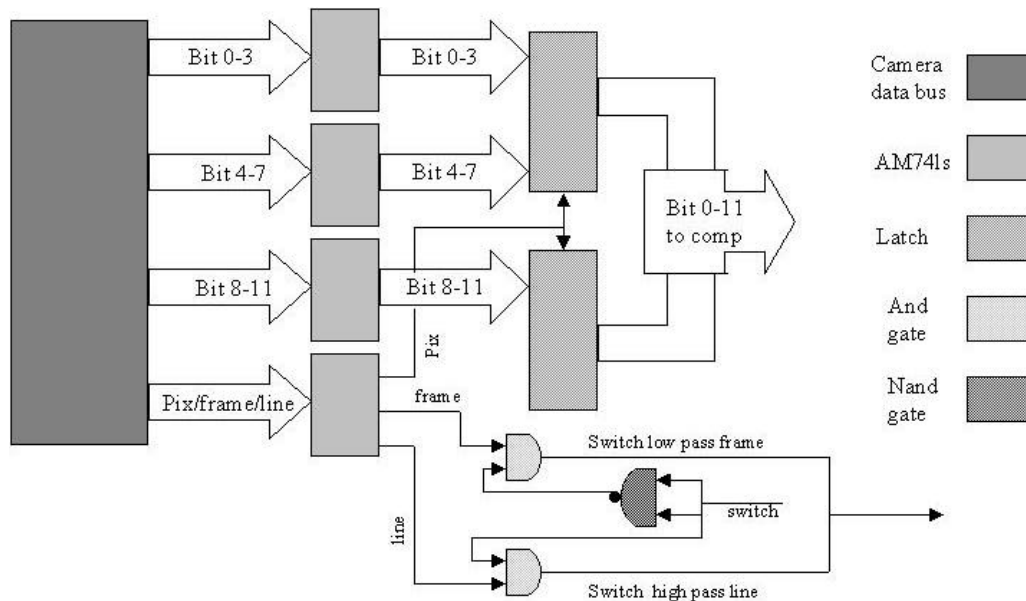
Figure 20. Digital Logic Circuit Diagram.

Data leaves the Evaluation board as 15 pairs of differential TTL. This is good to preserve the integrity of the data over distances but it can't be read into a computer in this

form. 4 **AM26LS32AC** Quad differential Line Receivers [Ref. 13] are utilized to

transform the 12 data lines and 3 control lines from differential TTL to the standard 0 – 5

V TTL signal.

The 12 lines of data are then sent to 2 **SN74F574** 8 bit flip-flops [Ref. 14]. Since

the data is available for only $3/8^{th}$ of the cycle time the flip-flops enable the data to be

latched and buffered making it available for the entire cycle time and allowing the data to

be read into the computer via the parallel port.

2.   Logic

Precise timing is necessary to ensure the latch is applied at the correct point in the

data cycle. As seen in Fig. 21 the video signal is only available for $3/8^{th}$ of the clock

period. Luckily the falling edge of the Pixel signal coincides with when the video data is

available. The latch needs a positive transition for its trigger, so the Pixel signal is

inverted by sending it through a NAND gate. The inverted Pixel signal undergoes a

positive transition and triggers the latch. The latch holds the video data until the next

Pixel signal, signifying the availability of new data, triggers the latch again.
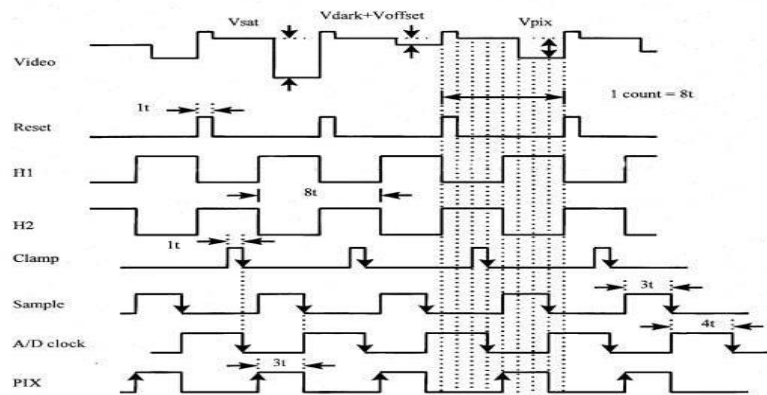
Figure 21. Eval Board Timing Diagram. From Ref. [7]

3. Computer Interface

The original plan to port data onto the computer involved building an 8-bit JDR prototype card [Ref. 10]. When installed into the computer expansion slot it would provide programmable addressing and internal data conditioning. In practice the card proved unwieldy and impossible to access using the NT operating system originally installed on the computer.

Using the proper drivers, NT allows access to the parallel port for import and export of data. This method proved nearly impossible to implement. Construction of a driver for NT involved extensive research [Ref. 18] and experience not available at NPS. NT is a network operating system whose main function is keeping users away from the hardware.

This made it necessary to change the operating system of the lab computer to Windows 98. Windows 98 allowed direct access to the hardware via commands in C or C++. Once access was gained the parallel port was configured for bi-directional data flow using the Extended Capabilities Port protocols [Refs. 11 & 12].

Pin #	Standard Use	Data Direction	Imager Use
1	Strobe	In/Out	Open
2	Data 0	In	Data 0
3	Data 1	In	Data 1
4	Data 2	In	Data 2
5	Data 3	In	Data 3
6	Data 4	In	Data 4
7	Data 5	In	Data 5
8	Data 6	In	Data 6
9	Data 7	In	Data 7
10	Ack	In	Data 10
11	Busy	In	Data 11
12	Paper-out	In	Data 9
13	Select	In	Data 8
14	Linefeed	Out	Gate Signal
15	Error	In	Read Status
16	Init	In/ Out	Open
17	Not-select	In/ Out	Open
18-25	Ground	Ground	Ground

Table 2. Parallel Port Line Designations. From Refs. [11 & 12]

When the port is properly set up 17 of the 25 lines become available for data import or export. 4 lines should never be used for input and 5 lines can never be used for output so max data lines are 13 in or 12 out. Since only one extra line to read data into the computer is available, another logic gate had to be set up.

4. Logic 2

The DREB provides 2 other signals that allow the handling software to gage where in the data stream it is. The timing diagram in Fig. 22 shows the Frame Signal pulled low to denote the beginning of a new frame and the Line signal pulsed high to show the beginning of each line. Utilizing an output line from the computer as a control, the last input line can be switched from the Line signal to the Frame signal. The control line is split and one of the splits is inverted using a NAND gate. The control line is sent

through an AND gate with the Frame signal. The inverted control line is sent through a different AND gate with the Line signal. The outputs of both AND gates are connected to the last input line. When the control line is high the Frame signal gets through, when the control line is low, the Line signal gets through.
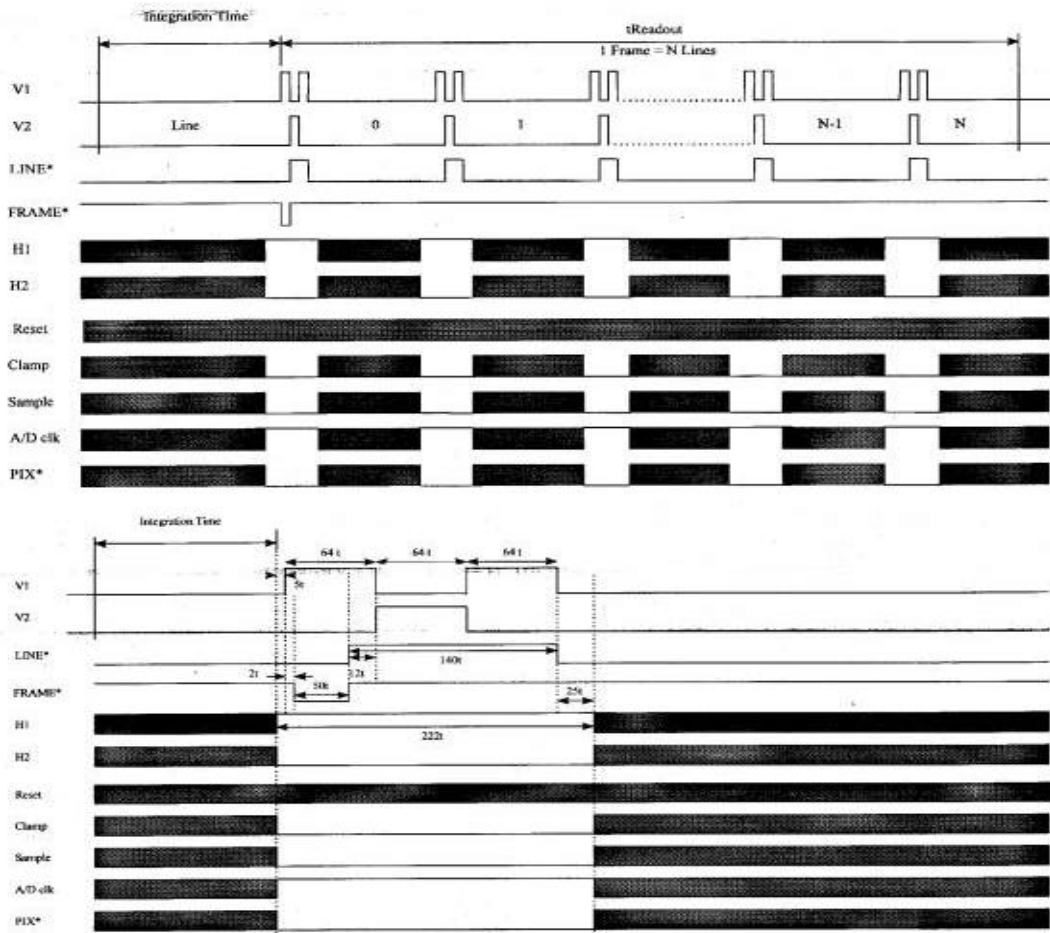

Figure 22. Eval Board Frame Timing Diagram.
From Ref. [7]

5. Software

a. C++

The working language of this bench-top prototype is C++ [Ref. 17]. C++ run on a DOS based operating system allows easy access to hardware controls. Once the techniques for initializing, reading to and writing from the parallel port are mastered, acquiring the data becomes easy. Storing the data involves using nested loops to set up a data array that matches the array of pixels to be read. The data can be stored to file in the same format. This enables it to be called up and viewed in the same format.

In practice there are some difficulties. The computer clock speed is 266 MHz but the actual speed of data acquisition is around 1 MHz. This maximum speed is achieved by using a nested loop that just reads data. All other functions are accomplished before or after the data acquisition loop in the code. Further improvements in speed may be accomplished by running the acquisition program on a machine completely dedicated to acquiring the data. Without other code running in the background the sampling speed could be significantly improved.

Large arrays of pixels require large variable arrays. These arrays may exceed the stack size available. This will preclude the program from running. The solution to this problem is dynamically allocating the variable array. This assigns memory from another, much larger location (see Appendix B for examples).

When C++ stores data in a file, its default is to store the data in ASCII format. This is slower and takes up more room than a binary file would. It also requires delimiter artifacts like spaces and carriage returns to be added. At this point in the

project, speed is not that important and there is plenty of memory space available. In addition, these artifacts make reading the data using other software easier.

A typical flow path for writing a C++ control code is as follows. Declare variables and constants. Initialize the parallel port. Wait for the Frame signal. Switch to the Line signal and wait for it. When the Line signal stops, start taking data. Once all data is taken, store the data. Quit the program.

b. Excel

Excel provides a quick easy way of looking at the actual number data before it gets processed into an image. The way to do this is to open excel and open the data file. Excel starts a Text Import Wizard to format and import the data in the file. It asks what kind of delimiters are used in the file. Click on spaces and click next then next and finally finish. The data array will be displayed.

Excel is most useful in conjunction with the Frame Grabber diagnostic mode of the DREB. This function outputs the Line number or the Pixel number instead of the image data to the data lines. Excel is the best way to check these numbers. Why these numbers are important will be covered later.

c. IDL

IDL is an image processing and data handling software package. Using the full power of this software would require intensive research and a lot of experimenting. Luckily IDL has a user-friendly image display Graphical Users Interface (GUI) that works well. This GUI is called Insight and allows display of data without resorting to the

integrated design language of the main IDL program. Once IDL is loaded import the image data by clicking on the import ASCII data icon in the upper left hand corner. Click on delimited then next then white space then next again. IDL reads the data from the file and stores it in variables by line. To get the data into array form, highlight all the lines of name and data type then click on group all then finish. The data will now be an IDL variable. Type in "insight" at the IDL prompt to launch GUI. Click new project then OK. Click IDL variable, check the box next to the data variable then OK. Highlight the data then close out with OK. To display the image, click on the image icon then click OK.

6.   Lenses

A variety of old but serviceable lenses were available in the lab. They varied in size from F = 14 mm with a 10 mm diameter, to F = 150 mm with a diameter of 25 mm. There was also a lens with F = 90mm and a diameter of 50 mm. These lens were adequate for acquiring images for testing purposes.

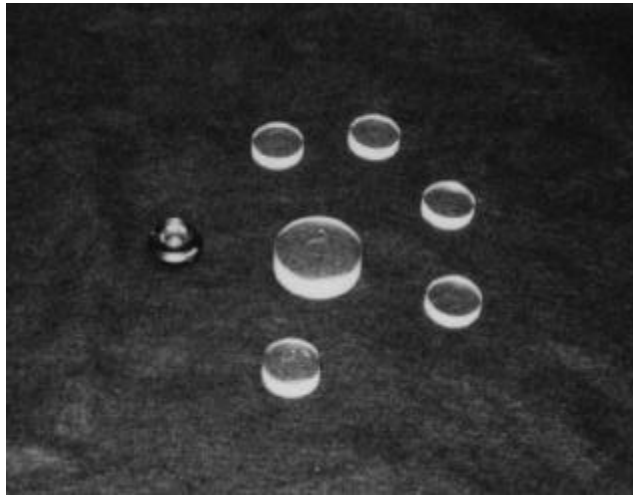Figure 23. Lenses Used to Acquire Data.

7.   Integrated System Operation

Once all the required pieces were together, integrating those pieces into a functioning whole could begin. The first step was building the logic gates and wiring the prototype board to allow data to flow from the DREB to the PC. Once a data path had been constructed, experimental runs could begin and the hardware configuration could be corrected and refined.

Initial data indicated a problem with a speed mismatch. The DREB was putting out data at 5 MHz based on its 40 MHz clock, and the computer could only read the data at <1 MHz. This conclusion was based on the numerical line data sent by the board in diagnostic mode and read using Excel. Based on timing diagrams, there were over 1000 pixel pulses per line. The computer was only reading 100 of them. Attempts to increase the sample speed of the PC by modifying the code produced modest results.

To allow different operating speeds, the board clock could be removed and a different timing signal could be provided. An ideal solution would be to send timing signals from the computer. In this way, the computer would always know where it was in the data cycle and would only need to read data lines. This configuration did not yield good data. A preliminary conclusion is that the computer is unable to send a clean enough signal for the ADC to operate correctly. Follow on tests revealed that the ADC has a minimum speed below which the output data becomes corrupted. This speed is 20 MHz–25 MHz.

When the Frame Grabber diagnostic mode was used the data came out exactly as they should. Since this information is placed into the output stream after the ADC this makes sense. This turned out to be a good method of verifying the timing diagrams. The

exact number of clock pulses per line and pixel could be verified. Additionally, when the Pixel, Line and Frame signals are read in as data in this configuration, their exact pulse length and periodicity can be calculated.

Following up on the theory that a clean signal would yield better data, a square wave function generator was hooked up in place of the clock. Experimental runs at 1, 10, 20 and 30 MHz were attempted with inconclusive results. Runs were done under varying amounts of illumination with varying integration times set. The expected cycling between high and low values were not seen. These runs were conducted with both of the C1 CCDs

The prototype was shown to the spacecraft engineers on staff at NPS and several suggestions were made. Electronic noise needed to be cleaned up on the power supplies. This was done using small capacitors. In addition, the latch needed to be in a high impedance state until right before it was read. This keeps garbage on the output side of the latch from affecting the data on the latch.

Once these modifications were complete, the CCD was removed and a controlled voltage source was attached to the board at the output of the CCD. New code was written to constantly scroll the output value of the ADC on the PC. This allowed any modification to voltage or board setting to be instantly obvious. For a set voltage, the output values were affected by the clock speed of the board. Any value below 20 MHz reduced the output voltage to zero. At a high clock speed the voltage changes changed the displayed output values as should be expected. Since these results did not match the experimental results with the two C1 CCDs, a C0 CCD was installed in the board. This CCD produced obvious changes in output values when exposed to a light source.

With an operational CCD installed in the board, the imager was aligned with a

test lens and a target (Fig. 24). Several test runs were necessary to ascertain the amount of

light and the integration time necessary to produce results. Poor quality images of the

target were obtained (Fig. 25). These images were of poor quality for two major reasons.

The speed mismatch detailed above only allows around 40 of the 712 pixels in the row to

be sampled. This compresses the data considerably.
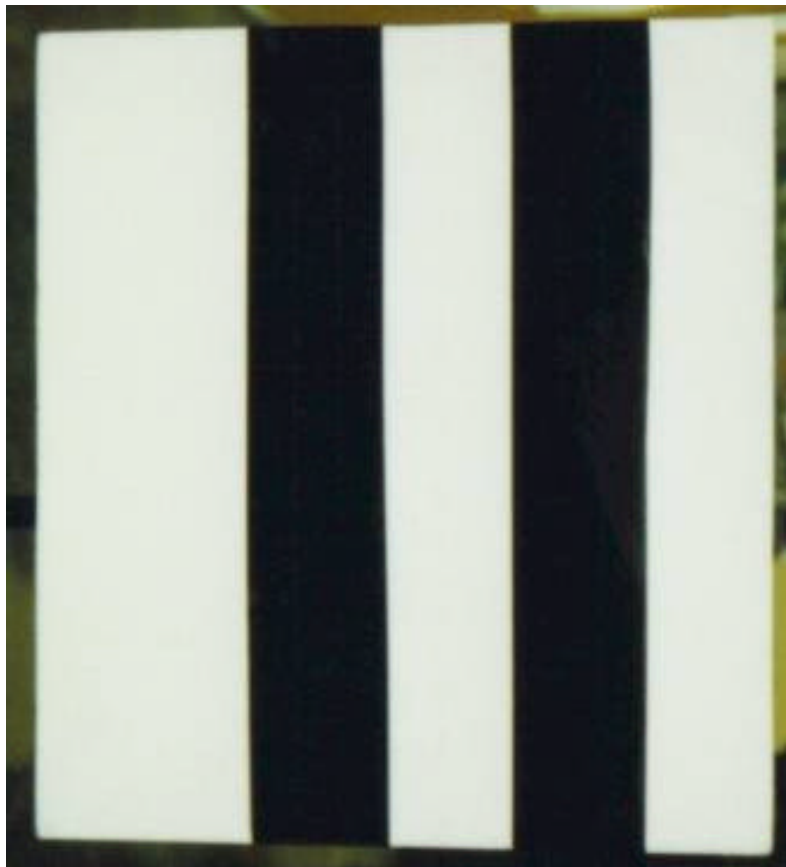
Figure 24. Picture of the Target to be Imaged
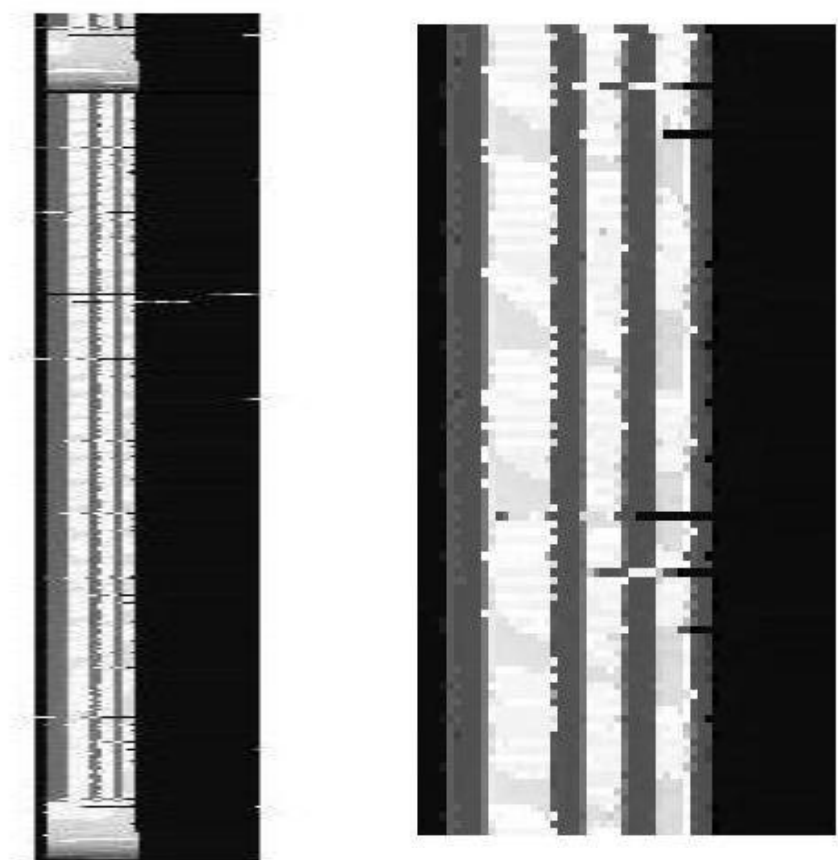
Figure 25. Data from the Imager.

The solution to this problem is to build a data buffer memory. This memory would need to be large enough to hold at least a frame worth of data. It could be sequentially loaded at a high rate, then sequentially read at a much lower rate. This would allow the PC to sample the data from every pixel.

The second problem is smearing. While the data lines are being systematically moved down the CCD so they can be read, the CCD is still collecting light. This light contaminates lines that would not normally have been in the path of that light. A bright light low on the CCD will be smeared all the way to the top of the CCD as the data gets clocked out.

The solution to this problem is to build a shutter device. The shutter is open during integration times and shut while the data is clocked out. The DREB provides a synchronization signal for shutter actuation, so timing would not be an issue.

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IV. CONCLUSIONS AND RECOMMENDATIONS

The objectives of this thesis were accomplished. Specifications for a space-based visible imager were investigated for validity and options for meeting or exceeding the specifications were tendered. Non-standard operating modes were investigated to cover the large dynamic range required of an Earth and auroral imager

The preliminary construction of a desk-top prototype is completed to the point of taking data. Further modifications are necessary to improve the quality of the data and the effectiveness of the imager.

Near the end of this project, the satellite bus program was cancelled. This does not diminish the importance of the imager project. The low cost associated with testing and constructing an imager makes it ideal for follow on work. In addition, the imager will be easy to integrate into any bus NPS builds in the future or any other bus the school has the opportunity to get a payload slot on.

A. ELECTRICAL ENGINEERING

There is a significant amount of electrical engineering work left to be done on this project. A shutter system must be developed to eliminate smearing and buffer memory needs to be integrated to match board to PC data rates. The CCD must be characterized as to actual sensitivity, and quantum efficiency. The hardware design must be matured away from the DREB and finalized. A Processor must be chosen and integrated into the design. Using a processor identical to those used on the spacecraft bus needs to be discussed with the spacecraft design engineers. Data compression techniques need to be discussed with

Dick Harkins. These schemes can be tested on the prototype. The various modes of operation need to be tested for feasibility.

B.   OPTICS AND FILTER TESTING

A sacrificial lens needs to be purchased and tested to destruction. Its optical properties and performance specifications need to be characterized. The lens must be thoroughly screened for non-space rated materials. Filters of the correct passband must be acquired and tested. The feasibility of laying multiple filters side by side over the CCD must be investigated.

C.   INTEGRATION AND TESTING

Once a flight model imager is constructed. It can be tested using the facilities at NPS. Shaker testing, and thermal and vacuum chamber tests are available. A test program will need to be developed and implemented to validate the imager design and improve the survivability of the imager on orbit.

APPENDIX A. "CHECK" C++ CODE

This code is designed to sample data coming in from the parallel port and display it on the computer monitor. This allows real time trouble-shooting of the logic and CCD setup without requiring a complete data run.

```cpp
#include <dos.h>
#include <fstream.h>
#include <stdio.h>
#include <iostream.h>
#include <conio.h>

#define PORT 0x378
#define DATA PORT
#define STATUS PORT+1
#define CONTROL PORT+2
#define ECRCONTROL 0x77A


void main(void) {

        _outp(ECRCONTROL, 0x21); //turn on bi direction
        _outp(CONTROL, 0x2b); // set data direction to read

        int q = 0;
        int p = 0;
        int i = 0;
        int input;
        int input2;

        _outp(CONTROL, 0x2a); //gate low reads frame

        while (q==0) {
              for (i=0;i<10;i++) {

                      _outp(CONTROL, 0x2b);// latch data
                      input = _inp(DATA); // Input data
                      input2 = _inp(STATUS); // input data
                      _outp(CONTROL, 0x2a);// reset latch

                      input2 = input2 & 0xf0; // convert to 12 bit
                      input2 = input2 << 4;   // data from 2 8 bit inputs
                      input2 = input2 + input;
                      cout << (input2 ^ 0x800) << "   ";
              }
                      cout << "\n";
                      for (i=0;i<1000000;i++) {} // counter slows output
        }


        return;
}
```

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APPENDIX B. "TEST2" C++ CODE

This code inputs a ROWS by COLUMN array of data into memory
and then saves that data to a file as declared in the
ofstream outfile line.

```cpp
#include <dos.h>
#include <fstream.h>
#include <stdio.h>
#include <iostream.h>
#include <conio.h>

#define PORT 0x378
#define DATA PORT
#define STATUS PORT+1
#define CONTROL PORT+2
#define ECRCONTROL 0x77A
#define ROWS 700
#define COLUMN 100

void main(void) {

        _outp(ECRCONTROL, 0x21); //turn on bi direction
        _outp(CONTROL, 0x2a); // set data direction to read

        int q = 0;
        int p = 0;
        int i = 0;
        int (*input)[COLUMN];
        int (*input2)[COLUMN];
        input = new int[ROWS][COLUMN];
        input2 = new int[ROWS][COLUMN];
        int flag = 1;
        ofstream outfile("data3.aaa");

        _outp(CONTROL, 0x2a); //gate low reads frame
        while (flag) {
                flag = (_inp(STATUS) & 0x08); // at beginning of frame
        }                                    // code moves on

        _outp(CONTROL, 0x28); //gate high reads line
```

```
for (q=0; q<ROWS;q++) {

        while (!flag) {
               flag = (_inp(STATUS) & 0x08);// reads start of line
        }
        while (flag) {
               flag = (_inp(STATUS) & 0x08);// reads end of line
        }

        for (p=0; p<COLUMN; p++) {

               _outp(CONTROL, 0x29);// enable latch
               input[q][p] = _inp(DATA); // get data
               input2[q][p] = _inp(STATUS);
               _outp(CONTROL, 0x28);// diable latch


}

for (q=; q<ROWS;q++) {
        for (p=0; p<COLUMN; p++) {

               input2[q][p] = input2[q][p] & 0xf0;
               input2[q][p] = input2[q][p] << 4;
               input2[q][p] = input2[q][p] + input[q][p];
               outfile << (input2[q][p] ^ 0x800) << " ";
        }
        outfile << "\n";
}
outfile.close();
return;
}
```

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